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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,656	PAEK, JONG SIK	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 4, 5, 7 and 8 are objected to because of the following informalities: In claims 4-5 and 7-8, line 1, "chip package" should be changed to "semiconductor package" for clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, lines 6-8, the phrase "at least one connecting bar portion extending from each of the pad portions of the outer set includes a bump land formed thereon" is unclear as to how connecting bar portion extending from the pad portions of the outer set includes a bump land formed thereon when they are previously identified as the pad portions of the inner set.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (PN 5,866,939).

Shin et al. discloses, as shown in Figures 1A, 10B, 11C and 19-21, a semiconductor package comprising:

a plurality of leads (2), each of the leads defining first and second surfaces;

a semiconductor (20) defining opposed first and second surfaces and including a plurality of input/output pads (not shown) disposed on the first surface thereof [Col. 15, lines 20-25, Col. 16, lines 38-43];

a plurality of conductive bumps (31) electrically connecting the input/output pads to the second surface of a respective one of the leads;

an encapsulant portion (40) covering the semiconductor chip, the conductive bumps, and the second surfaces of the leads such that at least portions of the first surfaces of the leads are exposed within the encapsulant portion.

With regard to claim 2, Shin et al. discloses the first surface of the semiconductor chip is disposed at a prescribed separation distance from the second surfaces of the leads [Figures 10B, 11C and 19-21].

With regard to claim 3, Shin et al. discloses the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof;

the third surface of each of the leads is covered by the encapsulant portion;

the first surface of each of the leads is exposed within the encapsulant portion to serve as an input/output terminal [Figures 10B, 11C and 19-21].

With regard to claim 4, Shin et al. discloses each of the leads includes a bump land formed at a prescribed region of the second surface thereof;

the conductive bumps are fused to respective ones of the bump lands of the leads [Figures 10B, 11C and 19-21].

With regard to claim 7, Shin et al. discloses each of the leads includes:

a pad portion (4);

at least one connecting bar portion integrally connected to the extending from the pad portion;

certain one of the leads each include a bump land formed on the second surface upon the pad portion thereof;

conductive bumps (31) are fused to respective ones of the bumps lands of the leads [Figures 1B, 10B, 11C and 19-21].

With regard to claim 8, Shin et al. discloses the pad portions (4) of the leads are segregated into an outer set and an inner set;

the pad portions (4) of the inner set each includes a bump land formed thereon;

at least one connecting bar portion (2a,2b) extending from each of the pad portions of the outer set includes a bump land formed thereon [Figures 1B, 10B, 11C and 19-21].

With regard to claim 9, Shin et al. discloses the first and second surfaces of each of the leads (2) are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surface thereof in opposed relation to that segment of the second surface which extends along the connecting bar portion (2a,2b);

the third surface of each of the leads is covered by the encapsulant portion (40);

the first surface of each of the leads extending along the pad portion thereof is exposed within the encapsulant portion to serve as an input/output terminal [Figures 1B, 10B, 11C and 19-21].

4. Claims 1-4 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Reference JP 7-312405 (of record).

Reference JP 7-312405 discloses, as shown in Figures 1-7, a semiconductor package comprising:

a plurality of leads (5), each of the leads defining first and second surfaces;

a semiconductor (3) defining opposed first and second surfaces and including a plurality of input/output pads (not shown) disposed on the first surface thereof;

a plurality of conductive bumps (2) electrically connecting the input/output pads to the second surface of a respective one of the leads;

an encapsulant portion (4) covering the semiconductor chip, the conductive bumps, and the second surfaces of the leads such that at least portions of the first surfaces of the leads are exposed within the encapsulant portion.

With regard to claim 2, Reference JP 7-312405 discloses the first surface of the semiconductor chip is disposed at a prescribed separation distance from the second surfaces of the leads [Figures 1-7].

With regard to claim 3, Reference JP 7-312405 discloses the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof;

the third surface of each of the leads is covered by the encapsulant portion;

the first surface of each of the leads is exposed within the encapsulant portion to serve as an input/output terminal [Figures 1-7].

With regard to claim 4, Reference JP 7-312405 discloses each of the leads includes a bump land formed at a prescribed region of the second surface thereof;

the conductive bumps are fused to respective ones of the bump lands of the leads [Figures 1-7].

With regard to claim 7, Reference JP 7-312405 discloses each of the leads includes:

a pad portion;

at least one connecting bar portion integrally connected to the extending from the pad portion;

certain one of the leads each include a bump land formed on the second surface upon the pad portion thereof;

conductive bumps (2) are fused to respective ones of the bumps lands of the leads [Figures 1-7].

With regard to claim 8, Reference JP 7-312405 discloses the pad portions (4) of the leads are segregated into an outer set and an inner set;

the pad portions of the inner set each includes a bump land formed thereon;

at least one connecting bar portion extending from each of the pad portions of the outer set includes a bump land formed thereon [Figures 1-7].

With regard to claim 9, Reference JP 7-312405 discloses the first and second surfaces of each of the leads (5) are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surface thereof in opposed relation to that segment of the second surface which extends along the connecting bar portion;

the third surface of each of the leads is covered by the encapsulant portion (4);

the first surface of each of the leads extending along the pad portion thereof is exposed within the encapsulant portion to serve as an input/output terminal [Figures 1-7].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (PN 5,866,939) in view of Baba et al. (PN 5,969,426).

With regard to claim 5, Shin et al. discloses the invention as claimed including the semiconductor package as cited in the rejection of claim 1. Shin et al. does not disclose each of the leads includes a protective layer formed on the second surface thereof other than for the prescribed region including the bump land. However, Baba et al. discloses each of the leads (7) includes a protective layer (21) formed on the second surface thereof other than for the prescribed region including the bump land. Note Figure 13 of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the leads of Shin et al. each includes a protective layer formed on the second surface thereof other than for the prescribed region including the bump land, such as taught by Baba et al., in order to prevent the diffusion of the bumps into the lead pattern and to control the configuration of the bumps.

With regard to claim 6, Shin et al. and Baba et al. disclose the protective layer is selected from the group consisting of polyimide [Col. 10, lines 9-11].

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reference JP 7-312405 (of record) in view of Baba et al. (PN 5,969,426).

With regard to claim 5, Reference JP 7-312405 discloses the invention as claimed including the semiconductor package as cited in the rejection of claim 1. Reference JP 7-312405 does not disclose each of the leads includes a protective layer formed on the second surface thereof other than for the prescribed region including the bump land. However, Baba et al. discloses each of the leads (7) includes a protective layer (21) formed on the second surface thereof other than for the prescribed region including the bump land. Note Figure 13 of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the leads of Reference JP 7-312405 each includes a protective layer formed on the second surface thereof other than for the prescribed region including the bump land, such as taught by Baba et al., in order to prevent the diffusion of the bumps into the lead pattern and to control the configuration of the bumps.

With regard to claim 6, Reference JP 7-312405 and Baba et al. disclose the protective layer is selected from the group consisting of polyimide [Col. 10, lines 9-11].

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The

examiner can normally be reached on Mon-Thurs 7:00-4:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

June 12, 2003

Hung Vu